Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A method for writing a memory module comprising:
providing a plurality of memory cells, wherein each memory cell stores 2-bit data and comprises a substrate, a first P-type doped region, a second P-type doped region, an oxide-nitride-oxide (ONO) layer, and a gate, the plurality of memory cells being arranged in matrix with the gates of the memory cells on the same row being connected to the same word line, the neighboring memory cells on the same column sharing the same P-type doped region, the first P-type doped region of the first memory cell in each column connected to a first transmission line in the same column, and the second P-type doped region of the last memory cell in each column connected to a second transmission line in the same column;
applying a first transmission line voltage to the first transmission line of the column which a memory cell to be written belongs to;
turning on a P-type channel of the memory cell between the memory cell to be written and the first transmission line of the column which the memory cell to be written belongs to, in order to transmit the first transmission

line voltage to the first P-type doped region of the memory cell to be written;

turning off the P-type channel of at least one memory cell between the memory cell to be written and the second transmission line of the column which the memory cell to be written belongs to;

applying a word line voltage to a word line connected to the memory cell to be written, in order to inject hot electrons on a junction between the substrate and the first P-type doped region of the memory cell to be written into a silicon nitride layer of the memory cell to be written by band-to-band tunneling (BTBT) injection;and

applying a substrate voltage to the substrates of the plurality of memory cells.

[c2] 2.The method of claim 1, wherein the first P-type doped region is for a drain of the memory cell, the second P-type doped region is for a source of the memory cell, the voltage of the first transmission line is 4V, and the voltage of the word line is 6V, so that hot electrons on the junction between the substrate and the drain of the memory cell to be written into the silicon nitride layer of the memory cell to be written by BTBT injection form a first-bit data.

[c3] 3.The method of claim 1, wherein the first P-type doped region is for a source of the memory cell, the second P-

type doped region is for a drain of the memory cell, the voltage of the first transmission line is 4V, and the voltage of the word line is 6V, so that hot electrons on the junction between the substrate and the drain of the memory cell to be written into the silicon nitride layer of the memory cell to be written by BTBT injection form a second-bit data.

[c4] 4.The method of claim 1, wherein the matrix is a NAND-array.

[c5] 5.The method of claim 1, wherein the first transmission line in each column is connected to the second transmission line in a previous column, the second transmission line in each column is connected to the first transmission line in a next column, in order to connect the plurality of memory cells serially to form a virtual ground.

[c6] 6.A method for reading a memory module comprising: providing a plurality of memory cells, wherein each memory cell stores 2-bit data and comprises a substrate, a first P-type doped region, a second P-type doped region, an ONO layer, and a gate, the plurality of memory cells being arranged in a matrix with the gates of the memory cells on the same row being connected to the same word line, the neighboring memory cells in the same column sharing the same P-type doped region, the

first P-type doped region of the first memory cell in each column being connected to a first transmission line in the same column, and the second P-type doped region of the last memory cell in each column being connected to a second transmission line in the same column;

applying a first transmission line voltage to the first transmission line of the column which a memory cell to be read belongs to;

applying a second transmission line voltage lower than the first transmission line voltage to the second transmission line of the column which the memory cell to be read belongs to;

applying a voltage equal to the first transmission line voltage to a word line connected to the memory cell to be read;

applying a voltage equal to the first transmission line voltage to the substrates of the plurality of memory cells; and

applying a word line voltage to the remaining word lines not connected to the memory cell to be read, in order to turn on a P-type channel of the memory cell, to transmit the second transmission line voltage to the second P-type doped region of the memory cell to be read, and to enlarge a depletion region between the second P-type doped region and the substrate of the memory cell to be read.

[c7] 7.The method of claim 6, wherein the first P-type doped region is for a drain of the memory cell, and the second P-type doped region is for a source of the memory cell.

[c8] 8.The method of claim 6, wherein the first P-type doped region is for a source of the memory cell, and the second P-type doped region is for a drain of the memory cell.

[c9] 9.The method of claim 6, wherein the first transmission line voltage is 0V, the second transmission line voltage is 1.5V, and the word line voltage is 3.3V.

[c10] 10.The method of claim 6, wherein the matrix is a NAND-array.

[c11] 11.The method of claim 6, wherein the first transmission line in each column is connected to the second transmission line in a previous column, the second transmission line in each column is connected to the first transmission line in a next column, in order to connect the plurality of memory cells serially to form a virtual ground.

[c12] 12.A method for erasing a memory module comprising: providing a plurality of memory cells, wherein each memory cell stores 2-bit data and comprises a substrate, a first P-type doped region, a second P-type doped region, an ONO layer, and a gate, the plurality of memory

cells being arranged in a matrix with the gates of the memory cells on the same row being connected to the same word line, the neighboring memory cells in the same column sharing the same P-type doped region, the first P-type doped region of the first memory cell in each column being connected to a first transmission line in the same column, and the second P-type doped region of the last memory cell in each column connected to a second transmission line in the same column;

applying a word line voltage to word lines of the plurality of memory cells;

applying a first transmission line voltage larger than the word line voltage to the first transmission line of the plurality of memory cells; and

applying a voltage equal to the first transmission line voltage to the substrates of the plurality of memory cells.

[c13] 13.The method of claim 12, wherein the word line voltage is 6V, and the first transmission line voltage is 6V.

[c14] 14.The method of claim 12, wherein the matrix is a NAND-array.

[c15] 15.The method of claim 12, utilizing Fowler-Nordheim tunneling to erase the electrons limited in the ONO layer.

[c16] 16.The method of claim 12, wherein the first transmis-

sion line in each column is connected to the second transmission line in a previous column, the second transmission line in each column is connected to the first transmission line in a next column, in order to connect the plurality of memory cells serially to form a virtual ground.